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(71) Applicant: KABUSHIKI KAISHA KENWOOD [JP/JP]; 14–6, Dougenzaka 1–chome, Shibuya–ku, Tokyo 150 (JP).

(72) Inventors: HORII, Akihiro; Room 108, 3–4719–5, Soubudai, Zama–shi, Kanagawa 228 (JP). SHIRAISHI, Kenichi; Room 407, 475–3, Kariba–cyo, Hodogaya–ku, Yokohama–shi, Kanagawa 240 (JP).

(74) Agents: OKABE, Masao et al.; 602 Fuji Building, 2–3, Marunouchi 3–chome, Chiyoda–ku, Tokyo 100 (JP).

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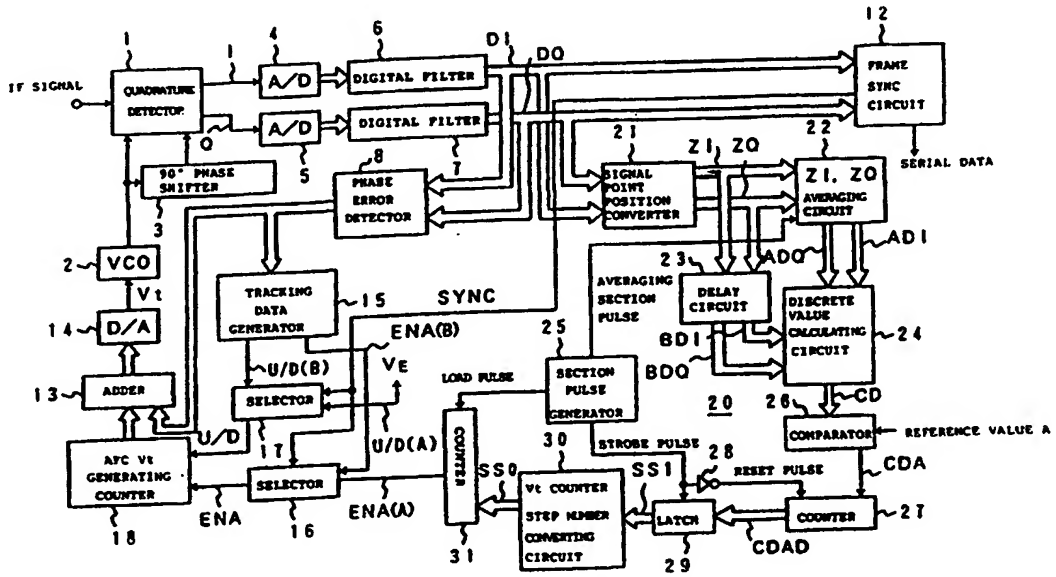

(57) Abstract

An auto frequency control circuit which can receive a desired signal in a shortest scanning time corresponding to a current reception C/N ratio. A reception C/N ratio is judged by a C/N ratio calculating unit (20) and a comparator (26) in accordance with signal point positions of a received and detected phase shift keying signal. A Vt counter step converting circuit (30) converts the judged reception C/N ratio into a predetermined scanning step frequency width preset for the judged reception C/N ratio in such a manner that a narrower scanning step frequency width is obtained for a lower reception C/N ratio. A frequency control voltage is generated in accordance with the converted scanning step frequency and applied to a VCO (2) to thereby sequentially scan an oscillation output of VCO (2) as a demodulation carrier.

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DESCRIPTION

AUTOMATIC FREQUENCY CONTROL CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an auto frequency control circuit to be used by a satellite broadcast receiver of a digital modulation type, and more particularly to an auto frequency control circuit for scanning a demodulation carrier frequency in a predetermined width.

2. Description of the Related Art

In this specification, a term "scanning" means frequency scanning for the regeneration of a demodulation carrier, and the term "scanning frequency width" means a range of central frequency change of a received signal which range is to be covered by a broadcast receiver. For example, a presently used CS digital satellite broadcast receiver has a scanning frequency width of about +/- 1.5 MHz.

After the power of a receiver of this type is turned on, scanning is performed. If a frame sync signal is received during this scanning, it is judged that the

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reception is in a frame sync state, and the scanning is stopped and a tracking state enters.

The structure of a receiver including a conventional auto frequency control (hereinafter abbreviated as AFC where applicable) circuit is partially shown in Fig. 6. The conventional AFC circuit will be described with reference to the receiver shown in Fig. 6. A received wave which was phase-shift keyed is converted into a predetermined frequency and input to a quadrature detector 1. The quadrature detector 1 is supplied with an oscillation output or demodulation carrier from a voltage controlled oscillator (hereinafter abbreviated as VCO) and an output or 90° shifted oscillation output from a 90° phase shifter 3. The frequency converted signal input to the quadrature detector 1 is therefore converted into I- and Q axes baseband signals.

The baseband signals are supplied to respective A/D converters 4 and 5 which convert them into discrete digital signals. The discrete digital signals are passed through respective digital filters 6 and 7 which output band-limited baseband signals DI and DQ. These baseband signals DI and DQ are supplied to a phase error detector 8 and to a frame synch circuit 12. The frame sync circuit 12 outputs serial data of the baseband signals DI and DQ and also outputs, when a frame synchronization is established,

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a high level frame sync signal (hereinafter abbreviated as SYNC signal where applicable).

The SYNC signal takes a high level when a frame synchronization is established. It is judged that the frame synchronization is established if a reception of a sync pattern at a constant period is detected at the head of frame data contained in a series of received data.

A frequency scanning data generator 10 generates scanning data which scans the oscillation frequency of VCO 2 in a scanning frequency width.

A phase error detector 8 detects a phase error in accordance with the input baseband signals DI and DQ. Phase error data representative of the detected phase error is supplied to a tracking data generator 9, which data is used as tuning data for VCO 2. The tracking data generator 9 generates tracking data in accordance with the supplied phase error data.

A selector 11 is supplied with the tracking data from the tracking data generator 9 and the scanning data from the frequency scanning data generator 10. If SYNC is a low level, i.e., if the frame synchronization is not established, the scanning data is selected by the selector 11, whereas if SYNC is a high level, i.e., if the frame synchronization is established, the tracking data is selected by the selector 11.

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The data output from the selector 11 and the tuning data are added together by an adder 13, and the output of the adder 13 is converted by a D/A converter 14 into an analog signal which controls the oscillation frequency of VCO 2. Namely, if the frame synchronization is not established, an addition signal of the scanning data selected by the selector 11 and the tuning data controls the oscillation frequency of VCO 2 to thereby carry out scanning.

If the frame synchronization is established during the scanning, an addition signal of the tracking data selected by the selector 11 and the tuning data controls the oscillation frequency of VCO 2 to thereby carry out tracking.

In the conventional AFC circuit, the frequency scanning data generator 10 is set with a scanning step frequency width in accordance with a capture range under the reception lowest conditions, e.g., at a reception limit ratio of carrier to noise (this ratio of carrier to noise is hereinafter abbreviated as C/N ratio, where applicable). It is therefore necessary to repeat the scanning (scanning frequency width)/(scanning step frequency width) times in order to scan the whole of the scanning frequency width.

In this specification, the term "scanning step frequency width" means a frequency change width per one

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scanning while the whole of the scanning frequency width is scanned.

In the above-described conventional AFC circuit, the scanning step frequency width for scanning the frequency of the demodulation carrier is narrower than the capture range used for the reproduction of the demodulation carrier, and in addition it is generally set to a value corresponding to a capture range determined from the reception limit C/N ratio. This poses the problem that it takes a constant scanning time to scan the whole of the scanning step frequency width, irrespective of a C/N ratio at that time.

It is an object of the present invention to provide an auto frequency control circuit capable of receiving a desired signal in a shortest scanning time corresponding to a current reception C/N ratio.

SUMMARY OF THE INVENTION

According to one aspect of the present invention, an auto frequency control circuit is provided which comprises: reception C/N ratio judging means for judging a reception C/N ratio in accordance with signal point positions of a received and detected phase shift keying signal; scanning step frequency width converting means for converting the reception C/N ratio judged by the reception C/N ratio judging means into a predetermined scanning step frequency

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width preset for the reception C/N ratio; and voltage converting means for converting the converted scanning step frequency width into a scanning voltage, wherein the converted scanning voltage is supplied to a voltage controlled oscillator as a frequency control voltage, an oscillation output of the voltage controlled oscillator being used as a demodulation carrier.

According to the auto frequency control circuit of this invention, reception C/N ratio judging means judges a reception C/N ratio in accordance with signal point positions of a received and detected phase shift keying signal, scanning step frequency width converting means converts the reception C/N ratio judged by the reception C/N ratio judging means into a predetermined scanning step frequency width preset for the reception C/N ratio, and voltage converting means converts the converted scanning step frequency width into a scanning voltage, wherein the converted scanning voltage is supplied to the voltage controlled oscillator as a frequency control voltage to sequentially scanning the scanning frequency width, and an oscillation output of the voltage controlled oscillator is sent as a demodulation carrier.

It is possible, for example, to use a broad scanning step frequency width if the reception C/N ratio is high. By changing the scanning step frequency width with the

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reception C/N ratio, it becomes possible to shorten a time required for receiving a desired signal.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram partially showing the structure of a receiver including an AFC circuit according to an embodiment of the invention.

Fig. 2 is a timing chart illustrating the operation of the AFC circuit of the embodiment.

Fig. 3 is a flow chart illustrating the operation of the AFC circuit of the embodiment.

Fig. 4 is a flow chart illustrating the detailed operation of Step S12 shown in the flow chart of Fig. 3.

Fig. 5 is an illustrative diagram showing the relationship among a reception C/N ratio, a receiver capture range, a scanning step frequency width and a Vt counter step number, respectively of the AFC circuit of the embodiment.

Fig. 6 is a block diagram partially showing the structure of a receiver including a conventional AFC circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

An embodiment of an auto frequency control

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circuit of this invention will be described. Fig. 1 is a block diagram partially showing a receiver including the auto frequency control circuit of the embodiment. In this embodiment, QPSK modulation is illustratively used as phase modulation. In Fig. 1, like elements to those of the conventional auto frequency control circuit shown in Fig. 6 are represented by using identical reference numerals.

Also in this receiver including the auto frequency control circuit of this embodiment, after the power of the receiver is turned on, scanning is performed. If a frame sync signal is received during this scanning, it is judged that the reception is in a frame sync state, and the scanning is stopped and a tracking state enters.

In the auto frequency control circuit of the embodiment, a received wave which was phase-shift keyed is converted into a predetermined frequency and input to a quadrature detector 1. The quadrature detector 1 is supplied with an oscillation output or demodulation carrier from a VCO 2 and an output or 90° shifted oscillation output from a 90° phase shifter 3. The frequency converted signal input to the quadrature detector 1 is therefore orthogonally detected to convert it into I- and Q axes baseband signals.

The baseband signals are supplied to respective A/D converters 4 and 5 which convert them into discrete digital

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signals. The discrete digital signals are passed through respective digital filters 6 and 7 which output band-limited baseband signals DI and DQ. These baseband signals DI and DQ are supplied to a phase error detector 8 and also to a frame sync circuit 12 which in turn outputs serial data of the baseband signals DI and DQ and also outputs a SYNC signal when a frame synchronization is established.

Frequency scanning by the auto frequency control circuit of this embodiment will be described first. In the frequency scanning by the auto frequency control circuit of this embodiment, a C/N ratio is calculated and the frequency scanning step is controlled in accordance with the calculated C/N ratio.

The baseband signals DI and DQ whose band widths were limited by the digital filters 6 and 7 are supplied to a C/N ratio calculating block 20 which determines a C/N ratio.

The C/N ratio calculating block 20 is constituted of a signal point position converting table 21, an averaging circuit 22, a delay circuit 23 and a discrete value calculating circuit 24. The signal point position converting table 21 is used for obtaining signal point position data ZI and ZQ by referring to the input baseband signals DI and DQ. The averaging circuit 22 is used for calculating average data ADI and ADQ during a predetermined

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period determined by an averaging section pulse shown in Fig. 2 at (a) and supplied from a section pulse generator 25, in accordance with the signal point position data ZI and ZQ obtained by the signal point position converting table 21. The delay circuit 23 is used for obtaining delay data BDI and BDQ by delaying the signal point position data ZI and ZQ obtained by the signal point position converting table 21, by a time required for averaging calculation. The discrete value calculating circuit 24 is used for obtaining discrete signal point positions in accordance with the average data ADI and ADQ and the delay data BDI and BDQ.

The signal point position converting table 21 will be described. In the case of QPSK modulation, a received signal (DI, DQ) has reference positions (0, 0), (0, 1), (1, 1) and (1, 0). The reference position (0, 0) is made to correspond to a first quadrant, (0, 1) is made to correspond to a second quadrant, the reference position (1, 1) is made to correspond to a third quadrant, and the reference position (1, 0) is made to correspond to a fourth quadrant. The reference position (0, 1) is rotated by 90° in the clockwise direction, the reference position (1, 1) is rotated by 180° in the clockwise direction, and the reference position (1, 0) is rotated by 90° in the counter-clockwise direction to make the reference positions

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correspond to the first quadrant. The received signal (DI, DQ) related to the first quadrant is converted into the signal point position data. In this manner, the signal point converting table 21 can be simplified.

In the C/N ratio calculating block 20, the input baseband signals DI and DQ are converted into signal point position data ZI_0, ZI_2,..., ZI_x and ZQ_0, ZQ_2,..., ZQ_x as shown in Fig. 2 at (b) and (c) by the signal point position converting table 21. The converted signal point position data ZI_0, ZI_2,..., ZI_x and ZQ_0, ZQ_2,..., ZQ_x is supplied to the averaging circuit 22 which obtains an average ADI of ZI_0, ZI_2,..., ZI_x and an average ADQ of ZQ_0, ZQ_2,..., ZQ_x during the period determined by the averaging section pulse, as shown in Fig. 2 at (d) and (e).

The signal point position data ZI_0, ZI_2,..., ZI_x and ZQ_0, ZQ_2,..., ZQ_x converted by the signal point position converting table 21 is delayed by the delay circuit 23 by the period required for the averaging calculation by the averaging circuit 22, to thereby obtain delay data BDI and BDQ as shown in Fig. 2 at (f) and (g). Discrete data CD such as shown in Fig. 2 at (h) is obtained in accordance with the average data ADI and ADQ obtained by the averaging circuit 22 and the delay data BDI and BDQ delayed by the delay circuit 23.

The discrete data CD may be obtained by the

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calculation described above, or may be obtained by searching the discrete data CD from a discrete data table which stores the average data ADI and ADQ and the delay data BDI and BDQ and the corresponding discrete data, by using the average data ADI and ADQ and the delay data BDI and BDQ as a search key.

The discrete data CD obtained by the discrete value calculating circuit 24 is supplied to a comparator 26 to compare it with a reference value A. If the discrete data has the value A or larger, a high level signal CDA is output from the comparator 26 and supplied to a counter 27. Therefore, while the high level signal CDA indicating that the discrete data CD has the value A or larger, is output, the counter 27 counts a clock pulse.

The counter 27 is reset by a reset pulse shown Fig. 2 at (i), the reset pulse being the averaging section pulse inverted by an inverter 28. The counter 27 once reset resumes its operation of counting the clock pulse and continues the counting while the high level signal CDA indicating that the discrete data CD has the value A or larger, is output.

The reference value A is set, for example, to "1000". Therefore, a count CDAD of the counter 27 corresponds to the number of discrete data CDA equal to "1000" or larger. In other words, the count CDAD corresponds to the total

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number of discrete data equal to "1000" or larger during the period preset by the section pulse generator 25.

As shown in Fig. 2 at (j), the counter 27 outputs counts $CDAD_0$, $CDAD_1$,... during respective averaging section pulse periods. The count CDAD of the counter 27 is supplied to a latch circuit 29 and latched in response to a strobe pulse shown in Fig. 2 at (k) having the same period as the averaging section pulse period.

The count CDAD latched by the latch circuit 29 is the total number of discrete data equal to the reference value A or larger during the period preset by the section pulse generator 25, and is proportional to a reception C/N ratio which is independent from the carrier reproduction. Therefore, the reception C/N ratio can be detected through table conversion or the like.

The count CDAD latched by the latch circuit 29 is supplied as data SS1 to a Vt counter step number converting circuit 30 which in turn converts the supplied data SS1 into a Vt counter step number SS0 at the timing shown in Fig. 2 at (l). For example, the Vt counter step number converting circuit 30 has a table which stores Vt counter step numbers SS0 and corresponding data SS1, and searches the Vt counter step number SS0 corresponding to the supplied data SS1 from the table by using the data SS1 as a search key.

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Next, the relationship between a discrete value and a C/N ratio will be described. As shown in Fig. 4, in the C/N ratio calculating block 20, discrete values of the signal point position data are calculated from the baseband signals DI and DQ (Step S21), the total number of discrete data equal to or larger than the reference value A ("1000") is counted by the counter 27 and latched by the latch circuit 29 (Step S22), and it is checked whether the total number is smaller than "100". If smaller than "100", it is determined that the reception C/N ratio is 13 dB or larger (Step S24).

If it is judged at Step S23 that the total number is not smaller than "100", it is checked whether the total number is smaller than "200" (Step S25). If the total number is "100" or larger, and smaller than "200", it is determined that the reception C/N ratio is about 11 dB (Step S26).

If it is judged at Step S25 that the total number is not smaller than "200", it is checked whether the total number is smaller than "300" (Step S27). If the total number is "200" or larger, and smaller than "300", it is determined that the reception C/N ratio is about 9 dB (Step S28). If it is judged at Step S27 that the total number is not smaller than "300", it is determined that the reception C/N ratio is about 7 dB or smaller (Step S29).

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As above, it is judged that the reception C/N ratio is 13 dB or larger if the total number is smaller than "100", that the reception ratio is about 11 dB if the total number is smaller than "200", that the reception C/N ratio is about 9 dB if the total number is equal to or larger than "200" and smaller than "300", and that the reception C/N ratio is equal to or smaller than 7 dB if the total number is equal to or larger than "300". The total number of discrete data for determining the reception C/N ratio described above was obtained from experiments, and it may change with modulation method and system used.

Optimizing the scanning in accordance with the reception C/N ratio obtained in the above manner will be described.

Fig. 5 shows the relationship between the reception C/N ratio judged in the above manner and the scanning step frequency width. In this relationship, the scanning step frequency width is set which satisfies the conditions that the capture range of a receiver actually measured is larger than the scanning step frequency width.

As described earlier, the scanning step frequency width is a frequency width to be changed at each scanning for scanning the whole of the scanning frequency width, and corresponds to the frequency width of the reproduction carrier output from VCO 2 during each scanning. If the

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tuning data supplied from the adder 13 does not change and is constant, the scanning step frequency width corresponds to a change in an output AFCCONT of an AFC Vt generating counter 18.

Therefore, if a change in the frequency of VCO 2 to be changed by one LSB bit supplied to the D/A converter 14 is represented by D, the scanning step frequency width is given by "D x (the output AFCCONT of the AFC Vt generating counter 18)".

In order to perform scanning at the scanning step frequency width corresponding to the reception C/N ratio, the AFC Vt generating counter 18 is therefore incremented by an amount of "(scanning step frequency width)/D" which is hereinunder called a Vt counter step number. In the AFC circuit of this embodiment, D is set to 45 Hz. As shown in Fig. 5, the Vt counter step numbers are set to 22, 44, 88 and 178 respectively at the reception C/N ratios of 7 dB, 9 dB, 11 dB and 13 dB.

The Vt counter step numbers were set to the above values because the Vt counter step number "22" x 45 Hz = 990 Hz is nearly equal to the scanning step frequency width of 1 kHz, the Vt counter step number "44" x 45 Hz = 1980 Hz is nearly equal to the scanning step frequency width of 2 kHz, the Vt counter step number "88" x 45 Hz = 3960 Hz is nearly equal to the scanning step frequency width of 4 kHz,

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and the Vt counter step number "178" x 45 Hz = 7920 Hz is nearly equal to the scanning step frequency width of 8 kHz.

Assuming that the reception center frequency change is +/- 1.5 MHz and so the scanning frequency width is 3 MHz, the whole scanning frequency width can be covered by the scanning step numbers of 3000, 1500, 750, and 375 respectively at the scanning step frequency widths of 1 kHz, 2 kHz, 4 kHz, and 8 kHz.

With the above settings, the scanning step frequency width is made narrower at the low reception C/N ratio, i.e., at a poor reception C/N ratio, because the capture range of the receiver is narrow and the reception signal cannot be captured, whereas the scanning step frequency width is made broader at the high reception C/N ratio, i.e., at a good reception C/N ratio, because the capture range of the receiver is broad and the reception signal can be captured.

With a conventional AFC circuit, the reception C/N ratio is not judged and the frequency scanning data is made constant to suffice for the worst reception C/N ratio. In contrast, with the AFC circuit of this embodiment, the scanning step frequency width is changed with the reception C/N ratio in such a manner that the scanning step frequency width is made broader as the reception C/N ratio becomes higher.

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The Vt counter step number converting circuit 30 refers to the supplied data SS1 and searches the Vt counter step number SS0 from the table which stores Vt counter step numbers SS0. The searched Vt counter step number SS0 is output to a counter 31 at a timing shown in Fig. 2 at (l).

The Vt counter step number SS0 is loaded in the counter 31 in response to a load pulse shown in Fig. 2 at (m) and output from the section pulse generator 25, and thereafter the counter 31 counts a clock pulse. The counter 31 outputs scanning data ENA (A) of a high level to a selector 16 until the count of the counter 31 reaches the Vt counter step number SS0.

A selector 17 is supplied with an up/down (U/D) (A) signal pulled up to the high level. During the scanning mode, i.e., while frame synchronization is not established, a SYNC signal supplied to the selectors 16 and 17 has a low level so that the selectors 16 and 17 select the scanning data ENA (A) and U/D (A) data and supply them to an AFC Vt generating counter 18.

The AFC Vt generating counter 18 counts up the clock pulse in a direction of scanning to a higher frequency, in response to the U/D (A) signal, while the scanning data ENA (A) is supplied. The count of the AFC Vt generating counter 18 and tuning data supplied from the phase error detector 8 are added together by an adder 13. Output data

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of the adder 13 is converted into an analog signal by a D/A converter 14. This analog signal is supplied to VCO 2 as a frequency control voltage to thereby control the oscillation frequency of VCO 2.

The U/D (A) signal may be pulled down to the low level. In this case, the AFC Vt generating counter 18 counts down the clock pulse in a direction of scanning to a lower frequency.

The frequency of a demodulation carrier reproduced as above is controlled by a frequency control voltage Vt supplied to VCO 2. This frequency control voltage of VCO 2 is output from the D/A converter 14. The relationship between addition data Vtd output from the adder 13 and input to the D/A converter 14 and the frequency of the reproduced demodulation carrier is made linear.

For example, if the Vt counter step number shown in Fig. 5 is set to "22", the frequency of the reproduced demodulation carrier can take an offset of +/- 1 kHz by incrementing or decrementing the data corresponding to "22" at the adder 13. As above, the scanning step number can be changed and optimized in accordance with the judged C/N ratio. If frame synchronization is established during the scanning, the SYNC signal takes the high level, At the same time when the SYNC signal takes the high level, the scanning state is switched to the tracking state.

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The phase error detector 8 is structured, for example, by a Costas operation circuit calculator having a conversion table. The phase error detector 8 calculates [(DI + DQ)·(DI - DQ)·DI·DQ] to detect a position error, i.e., phase error data, of the reception signal point positions of input baseband signals DI and DQ from the reference positions, for each quadrant. This phase error data is supplied to the adder 13 as the tuning data. A Costas loop for the reproduction of a basic demodulation carrier can therefore be formed, the loop being VCO 2 and 90° phase shifter 3 → quadrature detector 1 → A/D converter 4, 5 → digital filter 6, 7 → phase error detector 8 → adder → D/A converter 14 → VCO 2.

The phase error data is supplied to a tracking data generator 15 which generates tracking data. For example, the tracking data generator 15 has an averaging circuit and a comparator. The averaging circuit receives the phase error data and calculates an average value during a predetermined period, and the comparator compares the average value calculated by the averaging circuit with predetermined values on both sides of the center value (a value 0 in Costas operation) of Costas data, to check whether the average value is in the range between the predetermined values. If the average value is not in the range between the predetermined values, tracking data ENA

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(B) representative of a difference between the average value and one of the predetermined values is supplied to the selector 16 and an U/D (B) signal representative of the polarity of a difference between the average value and one of the predetermined values is supplied to the selector 17.

The selectors 16 and 17 are also supplied with the SYNC signal. If the SYNC signal is at the high level, the selector 16 selects the tracking data ENA (B) and the selector 17 selects the U/D (B) signal. The selected tracking data ENA (B) and U/D (B) signal are supplied to the AFC Vt generating counter 18 which counts up or down the tracking data ENA (B) in accordance with the U/D (B) signal.

The count of the AFC Vt generating counter 18 and the tuning data supplied from the phase error detector 8 are added together by the adder 13. The output data of the adder 13 is converted by the D/A converter 14 into an analog signal which is supplied to VCO 2 as the frequency control voltage to thereby control the oscillation frequency of VCO 2.

As above, if the tracking data generator 15 judges that the average value is in the range between the predetermined values and the frame synchronization is established, the frequency offset is finely adjusted by the tuning data. On the other hand, if the average value is

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not in the range between the predetermined values and the frame synchronization is not established, the frequency offset is finely adjusted by a sum of the tuning data and tracking data.

As described above, in the AFC circuit of this embodiment, the tuning data supplied to VCO 2 in the midst of the Costas loop for the regeneration of the demodulation carrier is updated by the scanning data if the frame synchronization is not established, whereas if the frame synchronization is established, the fine adjustment is performed by using the tracking data.

AFC control and tracking control will be described with reference to the flow chart shown in Fig. 3. If the SYNC signal is at the low level, i.e., if the frame synchronization is not established, the AFC circuit is in the scanning mode. In this mode, the Vt counter step number output from the Vt counter step number converting circuit 30 is loaded in the counter 31 which generates the scanning data ENA (A) having a time duration required for counting the clock pulses up to the Vt counter step number. The scanning data ENA (A) is supplied to the AFC Vt generating counter 18 which then counts up or down.

The scanning direction is selected by the U/D (A) signal. The data generated by the AFC Vt generating counter 18 is added to the tuning data by the adder 13, and

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the addition data is input to the D/A converter (Step S11). The above scanning operation is repeated (Steps S12, S13, S14 and S15) in accordance with the Vt counter step number satisfying the judged reception C/N ratio. The details of Step S12 are shown in the flow chart of Fig. 4. If a desired signal is received while Steps S12, S13, S14 and S15 are executed, the frame sync circuit 12 captures a sync signal contained in the received signal, and the data demodulation starts. At the same time, the SYNC signal takes the high level (Step S13).

When the SYNC signal takes the high level, the selectors 16 and 17 select the scanning data ENA (B) and U/D (B) signal to be replaced by the scanning data ENA (A) and U/D (A). The scanning operation is therefore stopped and the tracking operation starts in which the tracking data is added to the tuning data to finely adjust the frequency offset and repeat Steps starting from Step S12 (Step S14).

The scanning step frequency width of the AFC circuit depends on the capture range of the receiver. The capture range also changes with the reception C/N ratio. In a conventional AFC circuit, the scanning step frequency width is set in accordance with the capture range at the lowest target reception C/N ratio of the receiver so that it is set narrow irrespective of whether the reception C/N ratio

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is bad or good. Therefore, even at a good C/N ratio, the scanning is performed at a narrow scanning step frequency width and it takes a time to reproduce the demodulation carrier. In contrast, in the AFC circuit according to the embodiment of this invention, an optimum scanning step frequency width is selected in accordance with the judged reception C/N ratio. Accordingly, the capture range of the receiver is maintained properly and a desired signal can be received in a shortest scanning time corresponding to a current reception C/N ratio.

As described so far, according to the auto frequency control circuit of this invention, a reception C/N ratio is judged by processing the I and Q signals detected by the receiver, and the scanning step frequency width is changed with the judged C/N ratio. Accordingly, it is possible to receive a desired signal in a shortest scanning time corresponding to a current reception C/N ratio.

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CLAIMS

1. An auto frequency control circuit comprising:

reception C/N ratio judging means for judging a reception C/N ratio in accordance with signal point positions of a received and detected phase shift keying signal;

scanning step frequency width converting means for converting the reception C/N ratio judged by said reception C/N ratio judging means into a predetermined scanning step frequency width preset for the reception C/N ratio; and

voltage converting means for converting the converted scanning step frequency width into a scanning voltage,

wherein the converted scanning voltage is supplied to a voltage controlled oscillator as a frequency control voltage, an oscillation output of the voltage controlled oscillator being used as a demodulation carrier.

2. An auto frequency control circuit according to claim 1, wherein said reception C/N ratio judging means includes: signal point position converting means for converting the received and detected phase shift keying signal into signal point position data; averaging means for calculating an average value of the signal point position data; and discrete value calculating means for calculating a discrete

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value in accordance with the average value calculated by said averaging means and the signal point position data, wherein the reception C/N ratio is judged from the discrete value calculated by said discrete value calculating means.

3. An auto frequency control circuit according to claim 2, wherein said reception C/N ratio judging means includes delaying means for delaying the signal point position data converted by said signal point position converting means by a calculation time of said averaging means, wherein said discrete value calculating means calculates the discrete value in accordance with the average value calculated by said averaging means and the signal point position data delayed by said delaying means.

4. An auto frequency control circuit according to claim 1, wherein said reception C/N ratio judging means includes counting means for counting the number of occurrences of the discrete value equal to or larger than a predetermined reference value during a predetermined period, wherein the reception C/N ratio is judged from a count of said counting means.

5. An auto frequency control circuit according to claim 1, wherein said scanning step frequency width converting means

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converts the reception C/N ratio into a broad scanning step frequency width if the reception C/N ratio is high.

6. An auto frequency control circuit according to claim 1, wherein said scanning step frequency width converting means includes storage means for storing a scanning step frequency width corresponding to the judged reception C/N ratio, wherein the scanning step frequency width corresponding to the judged C/N ratio is read from said storage means by referring to the judged C/N ratio.

7. An auto frequency control circuit according to claim 1, further comprising switching means for switching the frequency control voltage supplied to the voltage controlled oscillator from the scanning voltage to a tracking voltage, if a frame sync signal is detected from a received signal.

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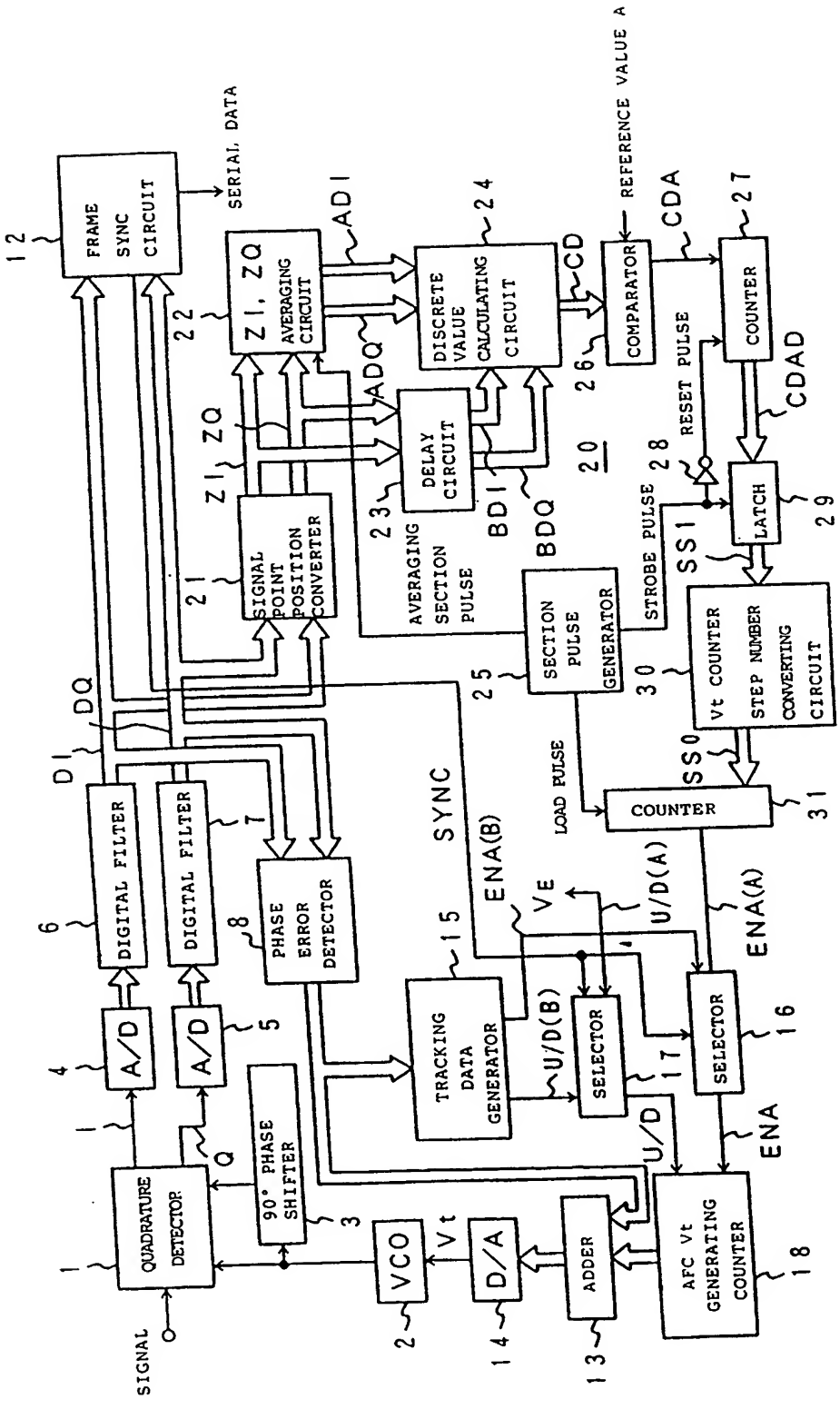
FRAME SYNC CIRCUIT
SERIAL DATA
Z1, ZQ AVERAGING CIRCUIT
ADI
ADQ
DISCRETE VALUE CALCULATING CIRCUIT
CD
COMPARATOR
REFERENCE VALUE A
CDA
COUNTER
CDAD
RESET PULSE
SIGNAL POINT POSITION CONVERTER
DELAY CIRCUIT
AVERAGING SECTION PULSE
BDI
BDQ
STROBE PULSE
SS1
LATCH
SECTION PULSE GENERATOR
Vt COUNTER STEP NUMBER CONVERTING CIRCUIT
SS0
LOAD PULSE
COUNTER
DIGITAL FILTER
DIGITAL FILTER
PHASE ERROR DETECTOR
SYNC
ENA(B)
Ve
U/D(A)
ENA(A)
A/D
A/D
90° PHASE SHIFTER
TRACKING DATA GENERATOR
U/D(B)
SELECTOR
SELECTOR
U/D
ENA
QUADRATURE DETECTOR
VCO
Vt
D/A
ADDER
AFC Vt GENERATING COUNTER
IF SIGNAL
DI
DQ
Q
1
2
3
4
5
6
7
8
12
13
14
15
16
17
18
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21
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31

Fig. 1

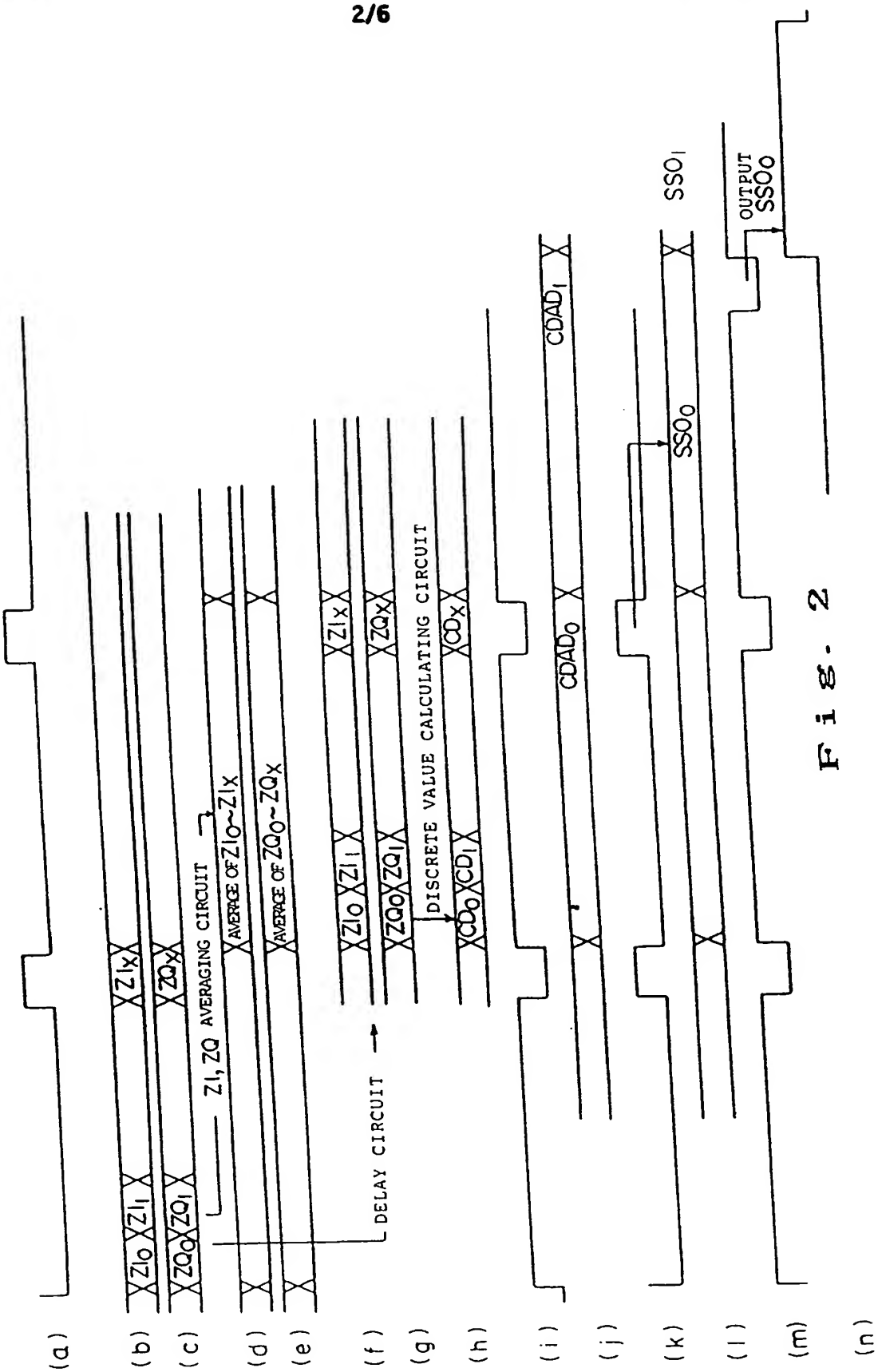

Fig. 2

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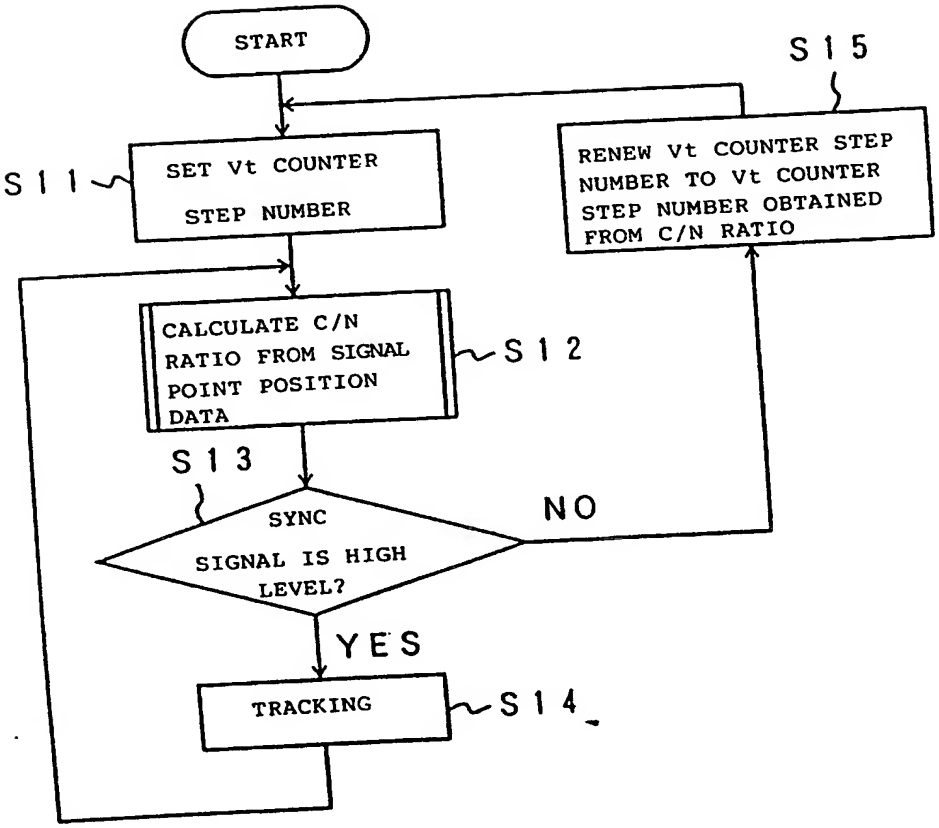
START
S11
SET Vt COUNTER STEP NUMBER
CALCULATE C/N RATIO FROM SIGNAL POINT POSITION DATA
S12
S13
SYNC SIGNAL IS HIGH LEVEL?
NO
YES
TRACKING
S14
S15
RENEW Vt COUNTER STEP NUMBER TO Vt COUNTER STEP NUMBER OBTAINED FROM C/N RATIO

Fig. 3

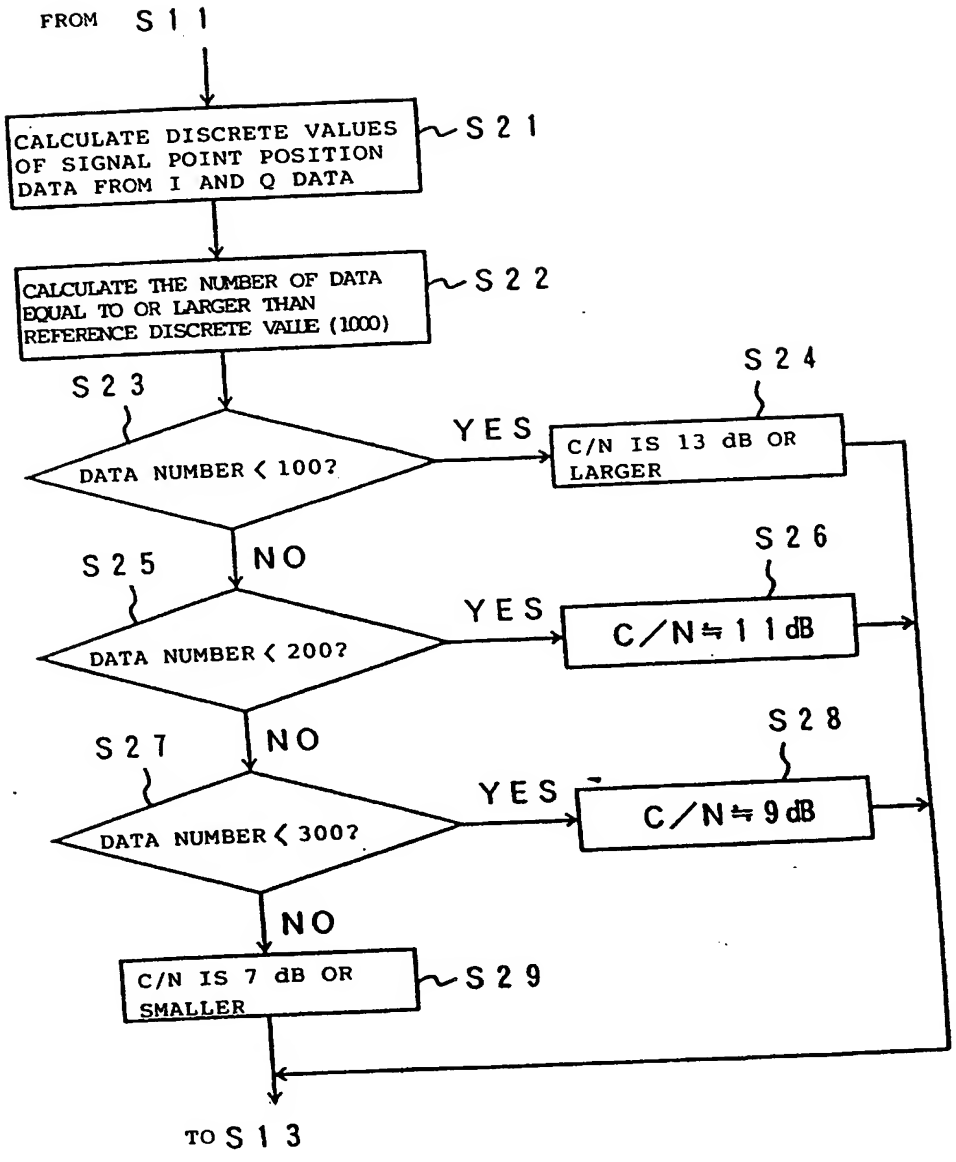
FROM S11
CALCULATE DISCRETE VALUES OF SIGNAL POINT POSITION DATA FROM I AND Q DATA
S21
CALCULATE THE NUMBER OF DATA EQUAL TO OR LARGER THAN REFERENCE DISCRETE VALUE (1000)
S22
S23
DATA NUMBER < 100?
YES
S24
C/N IS 13 dB OR LARGER
NO
S25
DATA NUMBER < 200?
YES
S26
C/N≒11dB
NO
S27
DATA NUMBER < 300?
YES
S28
C/N≒9dB
NO
C/N IS 7 dB OR SMALLER
S29
TO S13

Fig. 4

RECEPTION C/N RATIO (dB)	RECEIVER CAPTURE RANGE (KHz)	SCANNING STEP FREQUENCY WIDTH (KHz)	Vt COUNTER STEP NUMBER
7	1.2	1	22
9	2.8	2	44
11	4.5	4	88
13	8.5	8	176

Fig. 5

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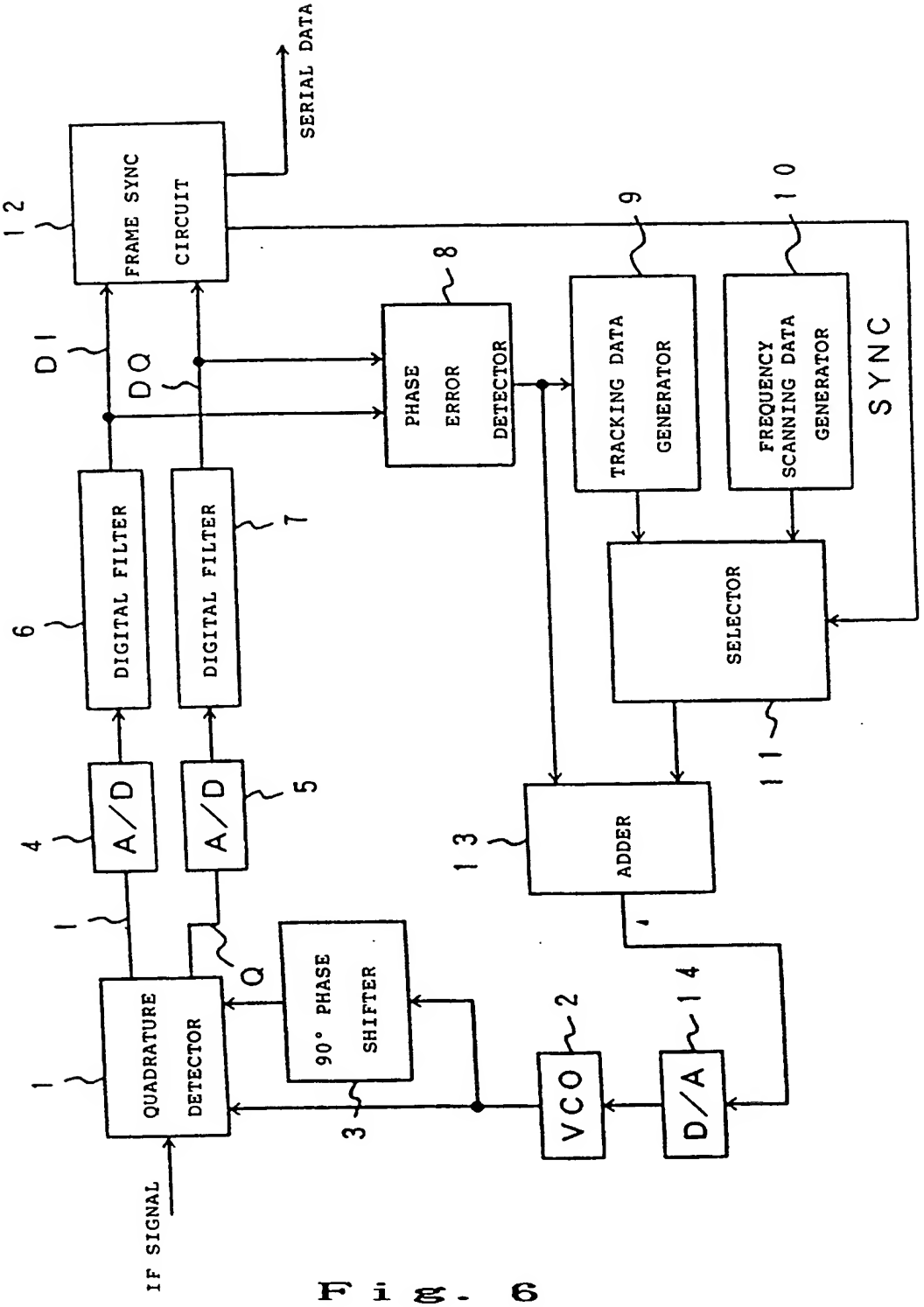
SERIAL DATA
FRAME SYNC CIRCUIT
12
DI
DQ
PHASE ERROR DETECTOR
8
TRACKING DATA GENERATOR
9
FREQUENCY SCANNING DATA GENERATOR
10
SYNC
DIGITAL FILTER
6
DIGITAL FILTER
7
SELECTOR
11
A/D
4
A/D
5
ADDER
13
I
Q
90° PHASE SHIFTER
3
QUADRATURE DETECTOR
1
VCO
2
D/A
14
IF SIGNAL

Fig. 6

INTERNATIONAL SEARCH REPORT

Int. ional Application No
PCT/JP 98/00354

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03J7/26 H03L7/12 H04L27/227

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03L H04L H03J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 281 412 A (WISSEL FRANK A ET AL) 28 July 1981 see column 8, line 23 - column 13, line 8; figures 5-8B	1,2,4
A	US 4 833 416 A (ATTWOOD STANLEY W) 23 May 1989 see column 2, line 19 - column 4, line 29; figure	1
A	US 5 289 506 A (KITAYAMA TAKAMITSU ET AL) 22 February 1994 see column 5, line 39 - column 7, line 37 see column 7, line 65 - column 8, line 31 see figures 6,9,18	1

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
15 April 1998	29/04/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Balbinot, H

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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 563 537 A (SETA MITSURU) 8 October 1996 see column 11, line 17 - column 13, line 40; figure 8	1
A	EP 0 445 522 A (PIONEER ELECTRONIC CORP) 11 September 1991 see column 2, line 42 - line 47 see column 3, line 17 - column 9, line 47; figures 1-6	1

2

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/JP 98/00354

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 5289506 A	22-02-94	JP 2087896 C	02-09-96
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		JP 8034488 B	29-03-96
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		JP 8034489 B	29-03-96
		JP 4306033 A	28-10-92
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		EP 0441593 A	14-08-91
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